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(54) Trench MOSFET having improved breakdown and on-resistance characteristics and process for manufacturing the same

(57) A trench MOSFET is formed in a structure which includes a P-type epitaxial layer overlying an N+ substrate. An N drain region is implanted through the bottom of the trench into the P-epitaxial layer, and after a diffusion step extends between the N+ substrate and the bottom of the trench. The junction between the N drain region and the P-epitaxial layer extends between the N+ substrate and a sidewall of the trench. In some embodiments the epitaxial layer can have a stepped doping concentration or a threshold voltage adjust implant can be added. Alternatively, the drain region can be omitted, and the trench can extend all the way through the P-epitaxial layer into the N+ substrate. A MOSFET constructed in accordance with this invention can have a reduced threshold voltage and on-resistance and an increased punchthrough breakdown voltage.

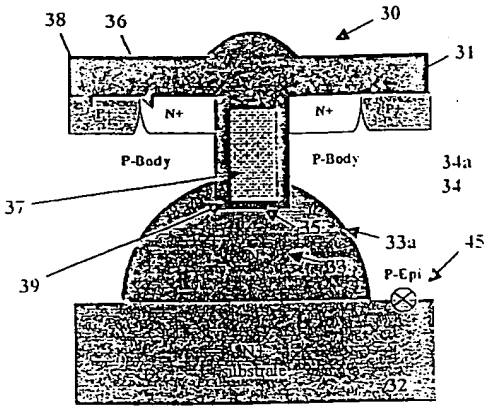

Figure 3

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Description

FIELD OF IN THE INVENTION

[0001] This invention relates to power MOSFETs and in particular to a trench-gated power MOSFET with superior on-resistance and breakdown characteristics. This invention also relates to a process for manufacturing such a MOSFET.

BACKGROUND OF THE INVENTION

[0002] A conventional trench-gated power MOSFET 10 is shown in the cross-sectional view of Fig. 1. MOSFET 10 is formed in an N+ semiconductor substrate 11, on which an N-epitaxial layer 12 is grown. A gate 13 is formed in a trench 14 which extends downward from the top surface of the N-epitaxial (N-epi) layer 12. The gate is typically made of polycrystalline silicon (polysilicon) and is electrically isolated from the N-epi layer 12 by an oxide layer 15. The voltage applied to the gate 13 controls the current flowing between an N+ source 16 and a drain 18, through a channel located adjacent the wall of the trench 14 in a P-body 17. Drain 18 includes the N-epi layer 12 and N+ substrate 11. A metal contact layer 19 makes electrical contact with the N+ source 16 and with the P-body 17 through a P+ body contact region 20. A similar metal contact layer (not shown) typically provides an electrical connection with the bottom side of the drain 18.

[0003] Ideally, the MOSFET would operate as a perfect switch, with infinite resistance when turned off and zero resistance when turned on. In practice, this goal cannot be achieved, but nonetheless two important measures of the efficiency of the MOSFET are its on-resistance and avalanche breakdown voltage (hereinafter "breakdown voltage"). Another important criterion is where the breakdown occurs. Since the drain is normally biased positive with respect to the source, the junction 21 is reverse-biased, and avalanche breakdown normally occurs at the corner of the trench, where the electric field is at a maximum. Breakdown creates hot carriers which can damage or rupture the gate oxide layer 15. It is therefore desirable to design the device such that breakdown occurs in the bulk silicon, away from the trench 14.

[0004] Another important characteristic of a MOSFET is its threshold voltage, which is the voltage that needs to be applied to the gate in order to create an inversion layer in the channel and thereby turn the device on. In many cases it is desirable to have a low threshold voltage, and this requires that the channel region be lightly doped. Lightly doping the channel, however, increases the risk of punchthrough breakdown, which occurs when the depletion region around the junction 21 expands so as to reach all the way across the channel to the source. The depletion region expands more rapidly when the body region is more lightly doped.

[0005] One technique for reducing the strength of the electric field at the corners of the trench and promoting breakdown in the bulk silicon away from the trench is taught in U.S. Patent No. 5,072,266 to Bulucea et al. (the "Bulucea patent") This technique is illustrated in Fig. 2, which shows a MOSFET 25, which is similar in MOSFET 10 of Fig. 1 except that a deep P+ diffusion 27 extends downward from the P-body 17 to a level below the bottom of the trench. Deep P+ diffusion 27 has the effect of shaping the electric field in such a way as to reduce its strength at the corner 29 of the trench.

[0006] While the technique of the Bulucea patent improves the breakdown performance of the MOSFET, it sets a lower limit on the cell pitch, shown as "d" in Fig. 2, because if the cell pitch is reduced too much, dopant from the deep P+ diffusion will get into the channel region of the MOSFET and increase its threshold voltage. Reducing the cell pitch increases the total perimeter of the cells of the MOSFET, providing a greater gate width for the current, and thereby reduces the on-resistance of the MOSFET. Thus, the net effect of using the technique of the Bulucea patent to improve the breakdown characteristics of the MOSFET is that it becomes more difficult to reduce the on-resistance of the MOSFET.

[0007] To summarize, the design of a power MOSFET requires that a compromise be made between the threshold and breakdown voltages and between the on-resistance and breakdown characteristics of the device. There is thus a clear need for a MOSFET structure that avoids or minimizes these compromises without adding undue complexity to the fabrication process.

SUMMARY OF THE INVENTION

[0008] In accordance with this invention a power MOSFET is formed in a semiconductor substrate of a first conductivity type which is overlain by an epitaxial layer of a second conductivity type. A trench is formed in the epitaxial layer. The power MOSFET also includes a gate positioned in the trench and electrically isolated from the epitaxial layer by an insulating layer which extends along the side walls and bottom of the trench. The epitaxial layer comprises a source region of the first conductivity type, the source region being located adjacent a top surface of the epitaxial layer and a wall of the trench; a base or body of the second conductivity type; and a drain region of the first conductivity type extending from the substrate to the bottom of the trench, a junction between the drain region and the body extending from the substrate to a side wall of the trench. The power MOSFET can optionally include a threshold adjust implant, and the epitaxial layer can include two or more sublayers having different dopant concentrations ("stepped epi layer")

[0009] In an alternative embodiment the trench extends through the entire epitaxial layer and into the

substrate, and there is no need for the drain region.

[0010] This invention also includes a process of fabricating a power MOSFET comprising providing a substrate of a first conductivity type; growing an epitaxial layer of a second conductivity type opposite to the first conductivity type on the substrate; forming a trench in the epitaxial layer; introducing dopant of the first conductivity type through a bottom of the trench to form a drain region, the drain region extending between the substrate and the bottom of the trench; forming an insulating layer along the bottom and a sidewall of the trench; introducing a conductive gate material into the trench; and introducing dopant of the first conductivity type into the epitaxial layer to form a source region, the drain region and the source region being formed under conditions such that the source region and drain region are separated by a channel region of the epitaxial layer adjacent the side wall of the trench. Alternatively, the trench can be made to extend through the epitaxial layer to the substrate.

[0011] A MOSFET of this invention has several advantages, including the following. Because the drain region is surrounded laterally by a second conductivity type portion of the epitaxial layer, more effective depletion occurs and more first conductivity type dopant can be put into the drain region, thereby decreasing the on-resistance of the MOSFET. Because the profile of the dopant in the channel region is relatively flat, the MOSFET can be made less vulnerable to punchthrough breakdown without increasing its threshold voltage. Since the second conductivity type portions of the epitaxial layer extend to the substrate except in the areas of the drain region, there is no need to form an additional second conductivity type layer for terminating the device. The separate mask for the deep diffusion of the Bulucea patent and the termination region can be eliminated. Eliminating the deep body diffusion of the Bulucea patent allows for increased cell density and reduced on-resistance.

[0012] A power MOSFET according to this invention can be fabricated in any type of cell geometry including, for example, closed cells of a hexagonal or square shape or cells in the form of longitudinal stripes.

BRIEF DESCRIPTION OF THE DRAWINGS

[0013]

Fig. 1 is a cross-sectional view of a conventional trench-gated MOSFET.

Fig. 2 is a cross-sectional view of a trench-gated MOSFET containing a deep diffusion to protect the gate oxide layer, as taught in the Bulucea patent.

Fig. 3 is a cross-sectional view of a trench MOSFET in accordance with the invention.

Fig. 4 is a cross-sectional view of a trench MOSFET in accordance with the invention containing a threshold adjust implant.

Figs. 5A-5L are cross-sectional views illustrating a process of fabricating the MOSFETs of Figs. 3 and 4.

Fig. 6 is a cross-sectional view of a trench MOSFET in accordance with the invention formed in stepped epitaxial layer.

Fig. 7 is a cross-sectional view of a trench MOSFET in accordance with the invention wherein the trench extends into the heavily-doped substrate.

Figs. 8A and 8B are graphs prepared using the computer simulation program SUPREME, showing the dopant concentrations in the MOSFET of Fig. 3 at vertical cross-sections through the channel region and the bottom of the trench, respectively.

Figs. 9A and 9B are graphs prepared using the computer simulation program MEDICI, showing the dopant concentrations in the MOSFET of Fig. 3 at vertical cross-sections through the channel region and the bottom of the trench, respectively.

Fig. 10 illustrates the depletion regions in the MOSFET of Fig. 3 under reverse bias conditions.

Figs. 11A and 11B are cross-sectional views illustrating the termination region of a MOSFET according to this invention and a conventional MOSFET, respectively.

Figs. 12A and 12B are doping profile graphs illustrating a threshold adjust implant and a body implant, respectively.

Fig 13A is a graph of the doping profile taken at a vertical cross-section through the channel of a conventional MOSFET having a diffused P-body in an N-epi region.

Fig 13B is a graph of the doping profile taken at a vertical cross-section through the channel of a MOSFET according to this invention having a P-epi layer and an N drain region.

DESCRIPTION OF THE INVENTION

[0014] A cross-sectional view of a power MOSFET in accordance with this invention is shown in Fig. 3. MOSFET 30 is formed in an N+ substrate 32 overlain by an epi layer 34, which is generally doped with a P-type impurity (hereinafter referred to as P-epi layer 34). N+ substrate 32 can have a resistivity of from 5×10^{-4} ohm-cm to 5×10^{-3} ohm-cm, for example, and P-epi layer 34 can be doped with boron to a concentration of from 1×10^{15} cm^{-3} to 5×10^{17} cm^{-3}. N+ substrate 32 is typically about 200 microns thick and epi layer 34 could be from 2 microns to 5 microns thick.

[0015] A trench 35 is formed in P-epi layer 34 and trench 35 contains a polysilicon gate 37. Gate 37 is electrically isolated from P-epi layer 34 by an oxide layer 39 which extends along the sidewalls and bottom of the trench 35. MOSFET 30 also includes an N+ source region 36, which is adjacent a top surface of the P-epi layer 34 and a sidewall of the trench 35, and a P+ body contact region 38. The remaining portion of the P-epi

layer 34 forms a P-type base or body 34A. Body 34A forms a junction with the N+ substrate 32 that is substantially coincident with the interface between the P-epi layer 34 and N+ substrate 32. A metal layer 31 makes electrical contact with N+ source region and with P-body 34A through P+ body contact region 38.

[0016] Further, in accordance with this invention an N drain region 33 extends between the N+ substrate 32 and the bottom of the trench 35. A junction 33A between N drain region 33 and P-body 34A extends between N+ substrate 32 and a sidewall of the trench 35. N drain region can be doped, for example, with phosphorus to a concentration of from 5×10^{15} cm^{-3} to 5×10^{17} cm^{-3}.

[0017] Fig. 8A is a graph of the doping concentration in MOSFET 30. The graph was prepared by the computer simulation program SUPREME and is taken at a vertical section through the channel region. The curves indicated show the doping concentrations of arsenic and boron, and the third curve shows the net doping concentration. Fig. 8B is a similar graph taken at a vertical section transecting the bottom of the trench. The horizontal axis in both graphs is the distance in microns below the surface of the P-epi layer; the vertical axis is the logarithm$_{10}$ of the doping concentration in atoms/cm^{-3}. Note that in Fig. 8A the concentration of boron, which is the background dopant in P-epi layer 34, is relatively flat and dominates in the channel region. The doping concentration of arsenic increases as one moves from the channel region into the source or the drain.

[0018] Figs. 9A and 9B are graphs of the doping concentration at the same sections, respectively, as Figs. 8A and 8B. Figs. 9A and 9B, however, were prepared using the computer simulation program MEDICI and show only the net doping concentration whether N-type or P-type.

[0019] The SUPREME and MEDICI simulations differ in that SUPREME considers only the doping concentrations at a single vertical cross-section, without taking into account the effect of dopants at other laterally displaced positions, while MEDICI takes into account all dopants in the two-dimensional plane of the drawing.

[0020] The following are among the advantages of MOSFET 30:

1. Avalanche breakdown will generally occur at the interface between the N+ substrate 32 and the P-epi layer 34, away from the trench (e.g., at the location designated 45 in Fig. 3). This avoids damage to the gate oxide layer from the hot carriers generated in the area of the breakdown.

2. The gate oxide at the corners of the trench, where the electric field reaches a maximum, is protected from rupture.

3. A higher punchthrough breakdown can be obtained for a given threshold voltage. The junction between the N drain region and the P-body extends downward to the N+ substrate. As shown in Fig. 10, when the MOSFET is reverse-biased the depletion regions extend along the entire junction, and as a result the depletion region in the area of the channel does not expand as quickly towards the source region (see arrows). This is the condition that causes punchthrough breakdown.

4. A higher punchthrough breakdown voltage can be obtained for a given threshold voltage. As shown in Fig. 13A, in a conventional MOSFET having a diffused body, the dopant concentration of the body falls off gradually as one approaches the N-epi (drift region). The threshold voltage is determined by the peak doping concentration $N_{A\ peak}$. The punchthrough breakdown voltage is determined by the total amount of charge $Q_{channel}$ in the channel region (represented by the area under the P-body curve in Fig. 13A). In a MOSFET of this invention, a doping profile of which is shown in Fig. 13B, the dopant profile of the P-epi layer is relatively flat. Therefore, $N_{A\ peak}$ can be the same while the total charge in the channel is greater, providing a higher punchthrough breakdown voltage.

5. Since there is no deep body diffusion in each cell (of the kind taught in the Bulucea patent) the cell pitch can be reduced without concern that additional P-type dopant will get into the channel region, raising the threshold voltage of the MOSFET. Thus the cell packing density can be increased. This reduces the on-resistance of the device.

6. In a conventional trench MOSFET a lightly-doped "drift region" is often formed between the channel and the heavily-doped substrate. The doping concentration in the drift region must be kept below a certain level because otherwise effective depletion is not obtained and the strength of the electric field at the corner of the trench becomes too great. Keeping the doping concentration in the drift region low increases the on-resistance of the device. In contrast, the N drain region 33 of this invention can be doped more heavily because the shape of N drain region 33 and the length of the junction between N drain region 33 and P-body 34A provide more effective depletion. A more heavily doped N drain region 33 reduces the on-resistance of the device.

7. As shown in Fig. 11A, there is no need for a separate P-type diffusion in the termination region of the MOSFET, since the P-epi layer extends to the N+ substrate except where the N drain regions are located. Fig. 11B shows the termination region of a conventional MOSFET which includes a P-type diffusion 110. The elimination of the P-type termination diffusion or field ring reduces the number of masking steps. For example, in the process illustrated in Figs. 5A-5L only five masking steps are required.

[0021] MOSFET 40, shown in Fig. 4, is an alterna-

tive embodiment which is similar to MOSFET 30 except that MOSFET 40 contains a threshold voltage adjust implant 42. Illustratively, such an implant would increase the threshold voltage of MOSFET 40 from 0.6 V to 1.0 V.

[0022] Figs. 5A-5L illustrate the steps of forming MOSFETs 30 and 40.

[0023] The process begins with N+ substrate 32 (Fig. 5A), on which P-epi layer 34 is grown by a well known process (Fig. 5B). A thin oxide layer 51 is then grown on the surface of P-epi layer 34 by heating in steam at 1150° C for about 50 minutes (Fig. 5C). Oxide layer 51 is masked and removed from the active area of the device (i.e., from the area where the active MOSFET cells are to be located) and it is left in the termination and gate pad areas.

[0024] A photoresist mask 52 is then formed on the surface of P-epi layer 34, and trench 35 is formed by a reactive ion etch (RIE) process. The process is terminated before the bottom of the trench reaches N+ substrate 32 (Fig. 5E)

[0025] Leaving photoresist mask 52 in place, phosphorus is implanted through the bottom of trench 35 at a dose of 1×10^{13} cm^{-2} to 1×10^{14} cm^{-2} and an energy of 300 keV to 3.0 MeV to produce N drain region 33 (Fig. 5F). To avoid significant diffusion of the phosphorus and the consequent expansion of N drain region 33, the thermal budget to which the structure is thereafter exposed is limited to the equivalent of about 950° C for 60 minutes, or the structure can be subjected to a rapid thermal anneal (RTA) at 1050° C for 90 seconds. In either case, N drain region 33 retains essentially the compact shape shown in Fig. 5F. Advantageously, in the cross-sectional view of Fig. 5F, at least 75% and preferably 90% of the N drain region 33 is located directly below the trench 35.

[0026] Alternatively, N drain region 33 can be formed by implanting the phosphorus at a lower energy of 30 keV to 300 keV (typically 150 keV), and diffusing the phosphorus by heating at 1050° C to 1150° C for 10 minutes to 120 minutes (typically 1100° C for 90 minutes), so that N drain region 33 expands laterally to a shape of the kind shown in Fig. 5G.

[0027] Using the high energy process results in an N drain region that is confined largely to the area directly below the trench and allows a smaller cell patch. It also is easier to control and provides greater throughput.

[0028] At the conclusion of the process, whether high energy or low energy, N drain region 33 extends from N+ substrate 32 to the bottom of trench 35, and the junction 33A between drain region 33 and P-body 34A extends from N+ substrate 32 to a sidewall of trench 35. If the low energy process is used, the junction 33A attains the form of an arc that is concave towards the drain region 33 (Fig. 5G).

[0029] Gate oxide layer 39 is then grown on the surface of P-epi layer 34 and on the bottom and sidewalls of trench 35, typically to a thickness of about 500 Å.

[0030] A polysilicon layer 53 is then deposited over the gate oxide layer 39, filling the trench 35 (Fig. 5H). In an N-channel MOSFET polysilicon layer 53 is typically doped with phosphorus to a concentration of 5×10^{19} cm^{-3}.

[0031] Polysilicon layer 53 is etched back so that its top surface is coplanar with the surface of P-epi layer 34. An oxide layer 54 is formed on the top of the gate by thermal oxidation or deposition (Fig. 5I).

[0032] Optionally, if the threshold voltage is to be adjusted, threshold voltage adjust implant 42 is formed. Implant 42 is formed, for example, by implanting boron through the surface of P-epi layer 34 (Fig. 5J) at a dose of 5×10^{12} cm^{-2} and at an energy of 150 keV, yielding a concentration of P-type atoms of 1×10^{17} cm^{-3} in the portion of P-epi layer 34 which will form the channel of the MOSFET. Fig. 12A is a graph showing a dopant profile of a vertical cross-section taken through the channel, showing a threshold adjust implant and indicating that the threshold adjust implant is typically located in an area of the channel just below the source region. The threshold voltage of the MOSFET is determined by the peak doping concentration $N_{A\ peak}$ of the threshold adjust implant. If the threshold voltage of the device does not need to be adjusted, this step can be omitted.

[0033] Alternatively, a body implant can be performed, as illustrated in the graph of Fig. 12B. The body implant is somewhat similar to the threshold adjust implant but the energy used is higher and as a result the body implant extends to a level near the junction between the P-epi layer and the N drain region. The threshold voltage of the MOSFET is determined by the peak doping concentration $N_{A\ peak}$ of the body implant.

[0034] N+ source regions 36 and P+ body contact regions 38 are formed at the surface of P-epi layer 34, using conventional masking and photolithographic processes (Fig. 5K). For example, N+ source regions can be implanted with arsenic at a dose of 5×10^{15} cm^{-2} and an energy of 80 keV, yielding a concentration of 1×10^{20} cm^{-3}; P+ body contact regions 38 can be implanted with boron at a dose of 1×10^{15} cm^{-2} and an energy of 60 keV, yielding a dopant concentration of 5×10^{19} cm^{-3}.

[0035] Finally, metal layer 31, preferably aluminum, is deposited on the surface of P-epi layer 34 in ohmic contact with N+ source regions 36 and P+ body contact regions 38.

[0036] Fig. 6 shows an alternative embodiment. MOSFET 60 is similar to MOSFET 30, but P-epi layer 34 is divided into sublayers Pepi1 and Pepi2. Using a well-known process, an epi layer having sublayers can be formed by varying the flow rate of the dopant gas while the epi layer is being grown. Alternatively, sublayer Pepi1 can be formed by implanting dopant into the upper portion of the epi layer 34.

[0037] The dopant concentration of sublayer Pepi1 can be either greater than or less than the dopant concentration of sublayer Pepi2. The threshold voltage and punchthrough breakdown of the MOSFET are a func-

tion of the doping concentration of sublayer Pepi1, while the breakdown voltage and on-resistance of the MOSFET are a function of the doping concentration of sublayer Pepi2. Thus, in a MOSFET of this embodiment the threshold voltage and punchthrough breakdown voltage can be designed independently of the avalanche breakdown voltage and on-resistance P-epi layer 34 may include more than two sublayers having different doping concentrations.

[0038] Fig. 7 shows another alternative embodiment. In MOSFET 70 drain region 33 is omitted, and trench 35 extends entirely through P-epi layer 34 into N+ substrate 32. This embodiment is particularly suitable for low-voltage (e.g., 5 V or less) MOSFETs.

[0039] While several specific embodiments of this invention have been described, these embodiments are illustrative only. It will be understood by those skilled in the art that numerous additional embodiments may be fabricated in accordance with the broad principles of this invention. For example, while the embodiments described above are N-channel MOSFETs, a P-channel MOSFET may be fabricated in accordance with this invention by reversing the conductivities of the various regions in the MOSFET.

Claims

1. A power MOSFET comprising:

   a semiconductor substrate of a first conductivity type;
   an epitaxial layer overlying the substrate, the epitaxial layer being generally of a second conductivity type opposite to the first conductivity type, a trench being formed in the epitaxial layer; and
   a gate positioned in the trench and electrically isolated from the epitaxial layer by an insulating layer which extends along a bottom and a sidewall of the trench;
   the epitaxial layer comprising:

   a source region of the first conductivity type, the source region being located adjacent a top surface of the epitaxial layer and the sidewall of the trench;
   a body of the second conductivity type; and
   a drain region of the first conductivity type extending between the substrate and the bottom of the trench, a junction between the drain region and the body extending between the substrate and the sidewall of the trench.

2. The MOSFET of Claim 1 wherein at least 75% of the drain region is located directly below the trench.

3. The MOSFET of Claim 1 wherein at least 90% of the drain region is located directly below the trench.

4. The MOSFET of Claim 1 wherein the shape of the junction between the drain region and the body is an arc that is concave in the direction towards the drain region.

5. The MOSFET of Claim 1 wherein the doping concentration in the drain region is between 5×10^{15} cm^{-3} and 5×10^{17} cm^{-3}.

6. The MOSFET of Claim 1 further comprising a threshold voltage adjust implant.

7. The MOSFET of Claim 1 further comprising a body implant.

8. The MOSFET of Claim 1 wherein the epitaxial layer comprises at least two sublayers, a first sublayer adjacent the surface of the epitaxial layer and a second sublayer between the first sublayer and the substrate, the first sublayer having a doping concentration different from the doping concentration of the second sublayer.

9. The MOSFET of Claim 8 wherein the doping concentration in the first sublayer is greater than the doping concentration in the second sublayer.

10. The MOSFET of Claim 8 wherein the doping concentration in the first sublayer is lower than the doping concentration in the second sublayer.

11. The MOSFET of Claim 8 wherein an interface between the first sublayer and the second sublayer intersects the sidewall of the trench.

12. A power MOSFET comprising:

    a semiconductor substrate of a first conductivity type;
    an epitaxial layer overlying the substrate, a trench being formed in the epitaxial layer; and
    a gate positioned in the trench and electrically isolated from the epitaxial layer by an insulating layer which extends along a bottom and a sidewall of the trench;
    the epitaxial layer comprising:

    a source region of the first conductivity type, the source region being located adjacent a top surface of the epitaxial layer and the sidewall of the trench;
    a body of the second conductivity type, the body forming a junction with the substrate substantially coincident with the interface between the epitaxial layer and the sub-

strate; and

a drain region of the first conductivity type extending between the substrate and the bottom of the trench.

13. The MOSFET of Claim 12 wherein a junction between the drain region and the body extends between the substrate and the sidewall of the trench

14. A power MOSFET comprising:

a semiconductor substrate of a first conductivity type;

an epitaxial layer overlying the substrate, the epitaxial layer being generally of a second conductivity type opposite to the first conductivity type;

a trench extending from a surface of the epitaxial layer, through the epitaxial layer and into the substrate;

a gate positioned in the trench and electrically isolated from the epitaxial layer by an insulating layer which extends along a bottom and a sidewall of the trench; and

a source region of the first conductivity type in the epitaxial layer, the source region being located adjacent a top surface of the epitaxial layer and the sidewall of the trench.

15. A process of fabricating a power MOSFET comprising:

providing a substrate of a first conductivity type;

growing an epitaxial layer of a second conductivity type opposite to the first conductivity type on the substrate;

forming a trench in the epitaxial layer;

introducing dopant of the first conductivity type through a bottom of the trench to form a drain region, the drain region extending between the substrate and the bottom of the trench;

forming an insulating layer along the bottom and a sidewall of the trench;

introducing a conductive gate material into the trench; and

introducing dopant of the first conductivity type into the epitaxial layer to form a source region, the drain region and the source region being formed under conditions such that the source region and drain region are separated by a channel region of the epitaxial layer adjacent the sidewall of the trench.

16. The method of Claim 15 wherein introducing dopant of the first conductivity type through a bottom of the trench is performed by implanting dopant at an energy of from 300 keV to 3.0 MeV.

17. The method of Claim 16 wherein the thermal budget following the formation of the drain region is limited to the equivalent of about 950° C for 60 minutes.

18. The method of Claim 15 comprising applying a thermal budget of greater than the equivalent following the formation of the drain region.

19. The method of Claim 15 further comprising introducing a threshold voltage adjust implant into the epitaxial layer.

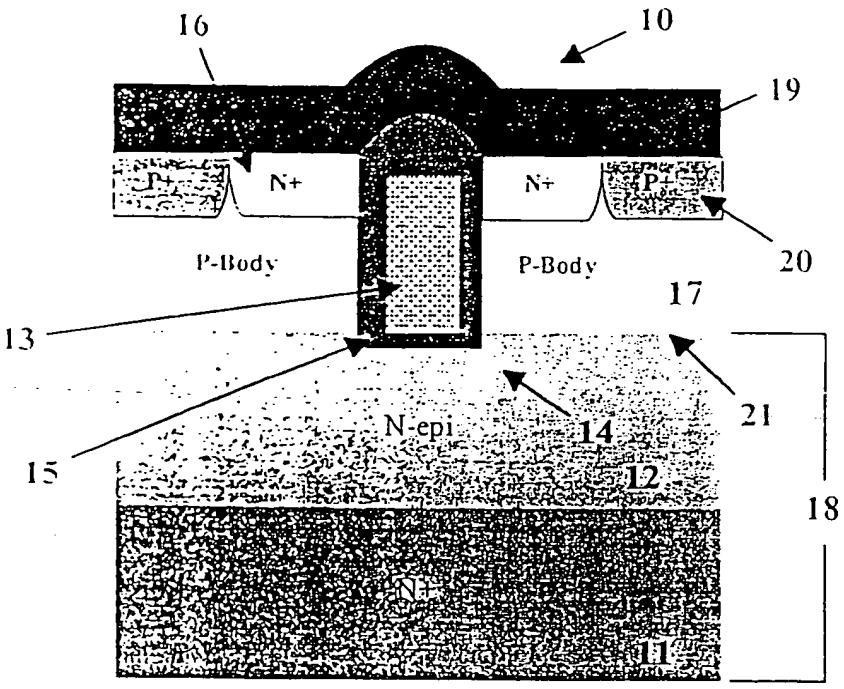

Figure 1

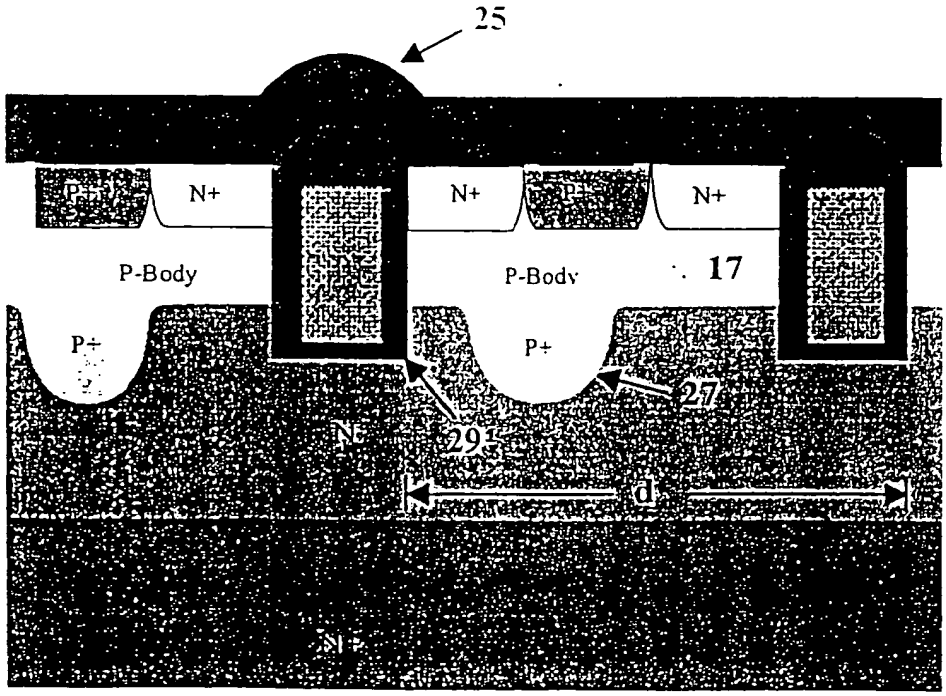

Figure 2

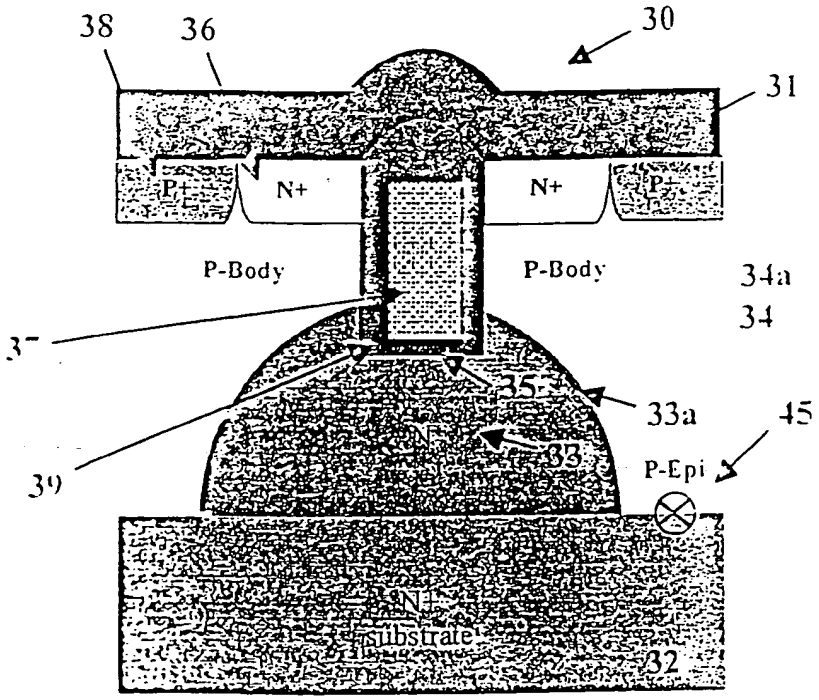

Figure 3

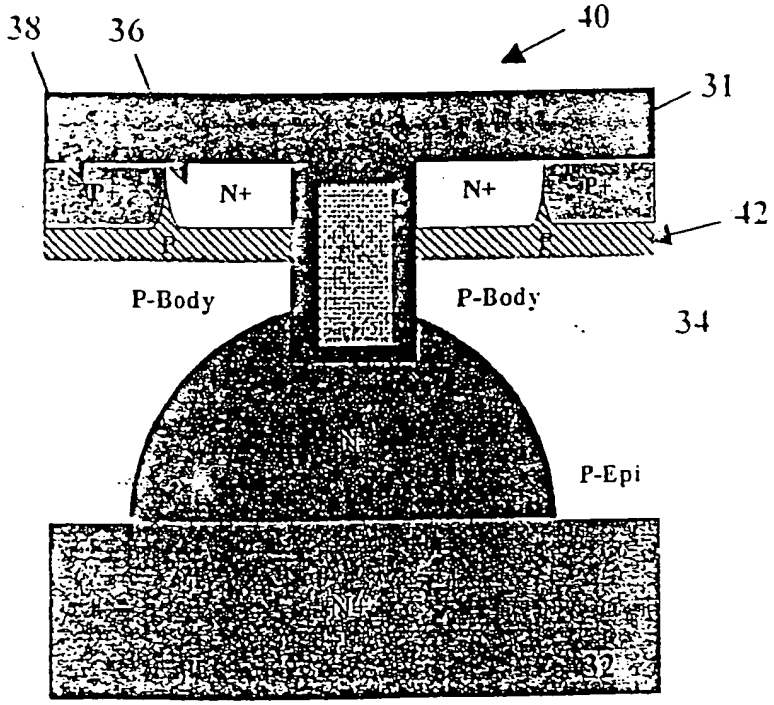

Figure 4

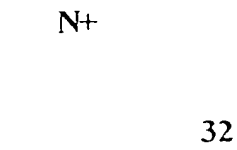

Figure 5a A

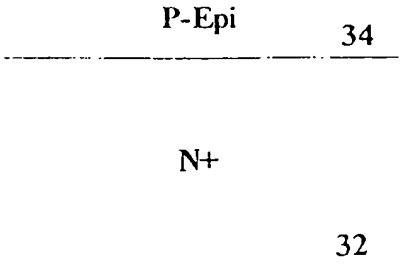

Figure 5d D

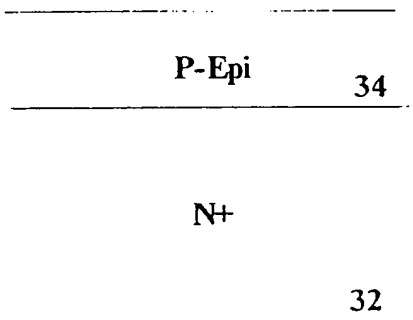

Figure 5b B

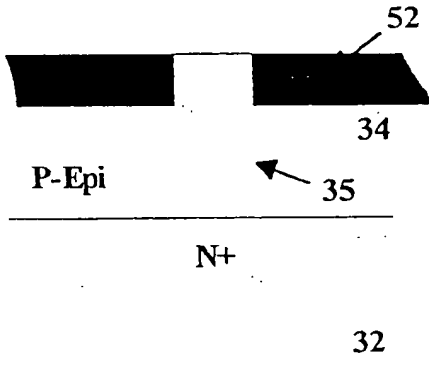

Figure 5e E

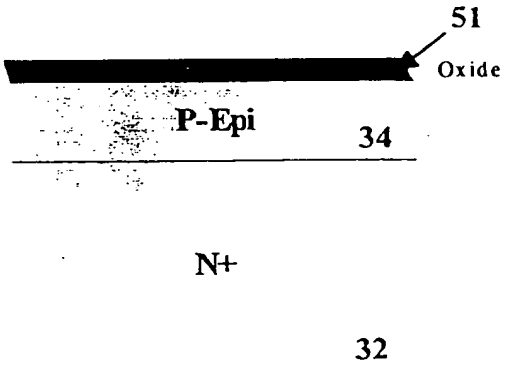

Figure 5c C

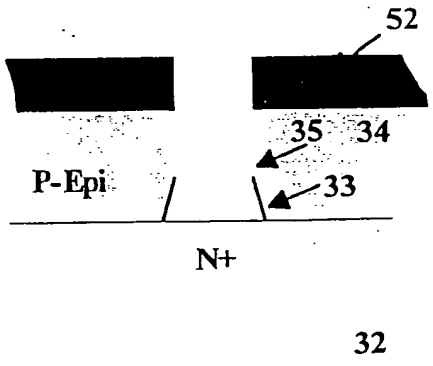

Figure 5f F

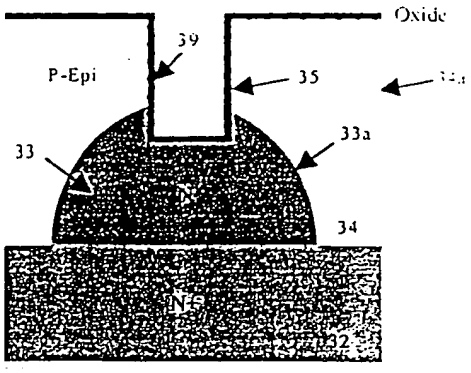

Figure 5G

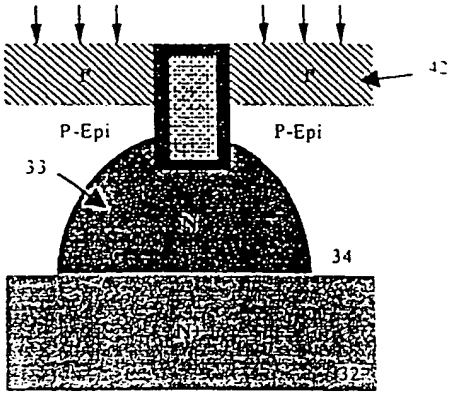

Figure 5J

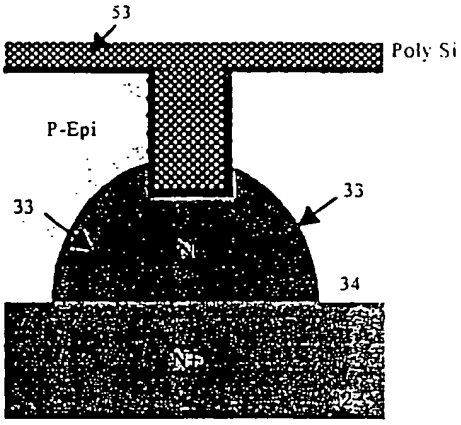

Figure 5H

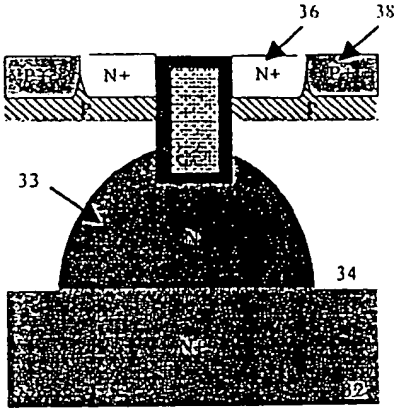

Figure 5K

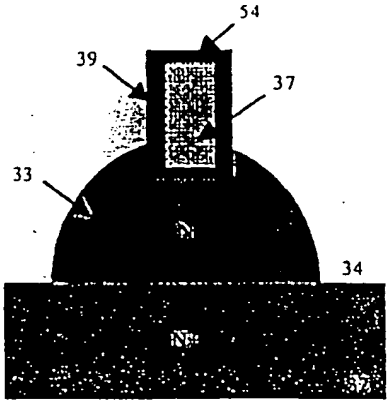

Figure 5I

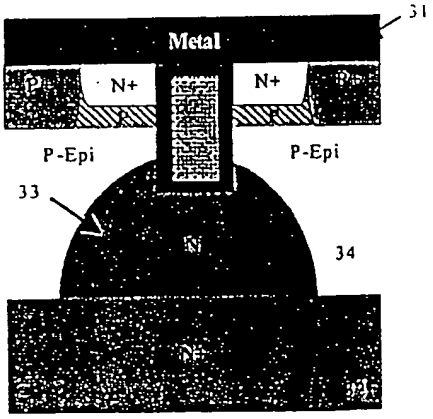

Figure 5L

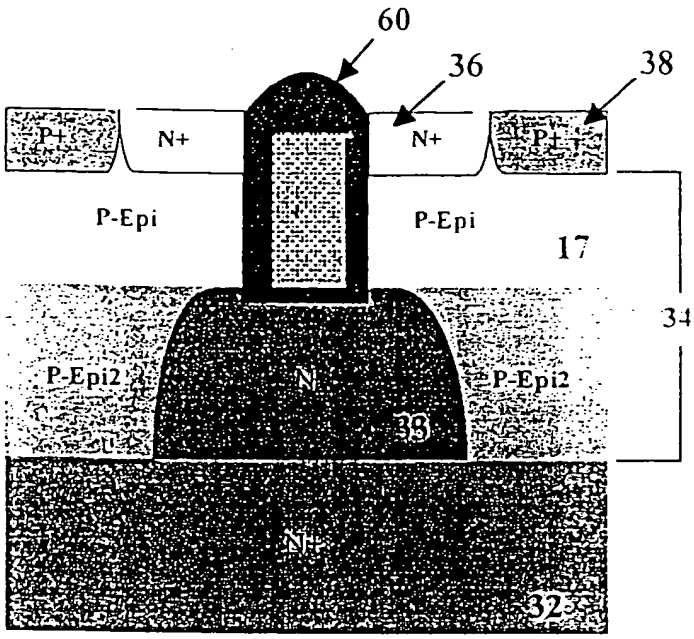

Figure 6

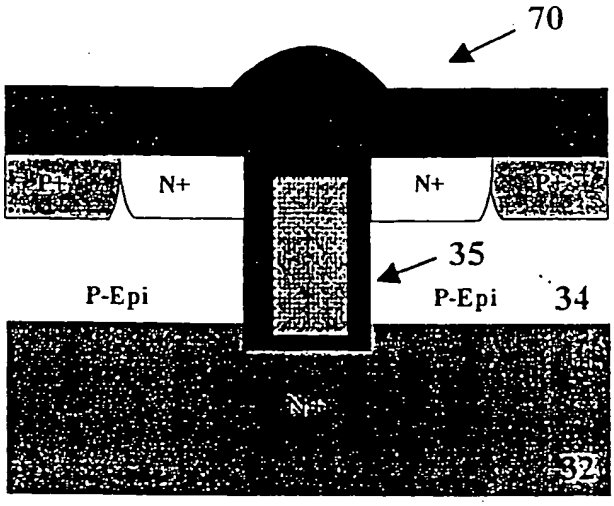

Figure 7

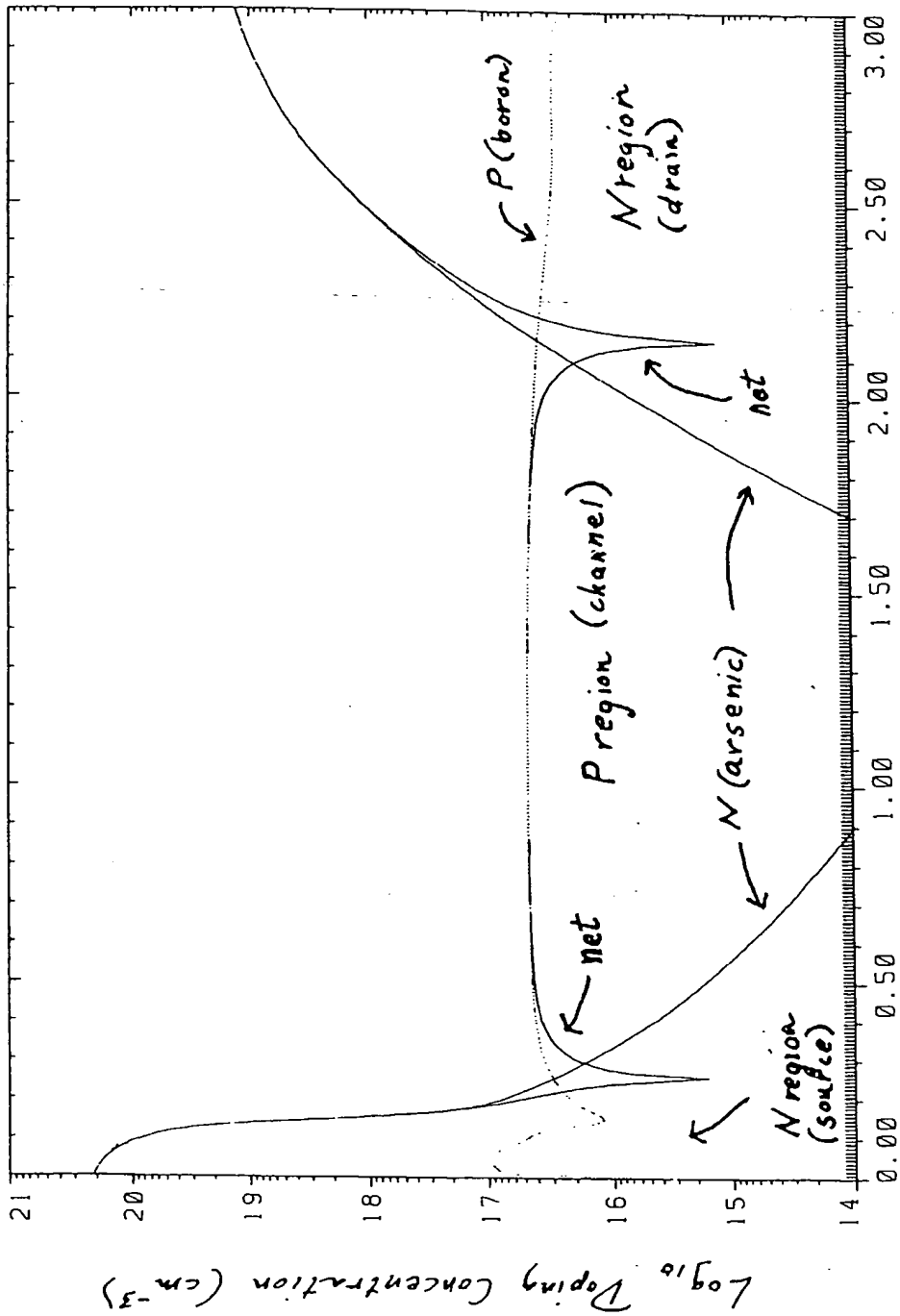

Fig. 8A

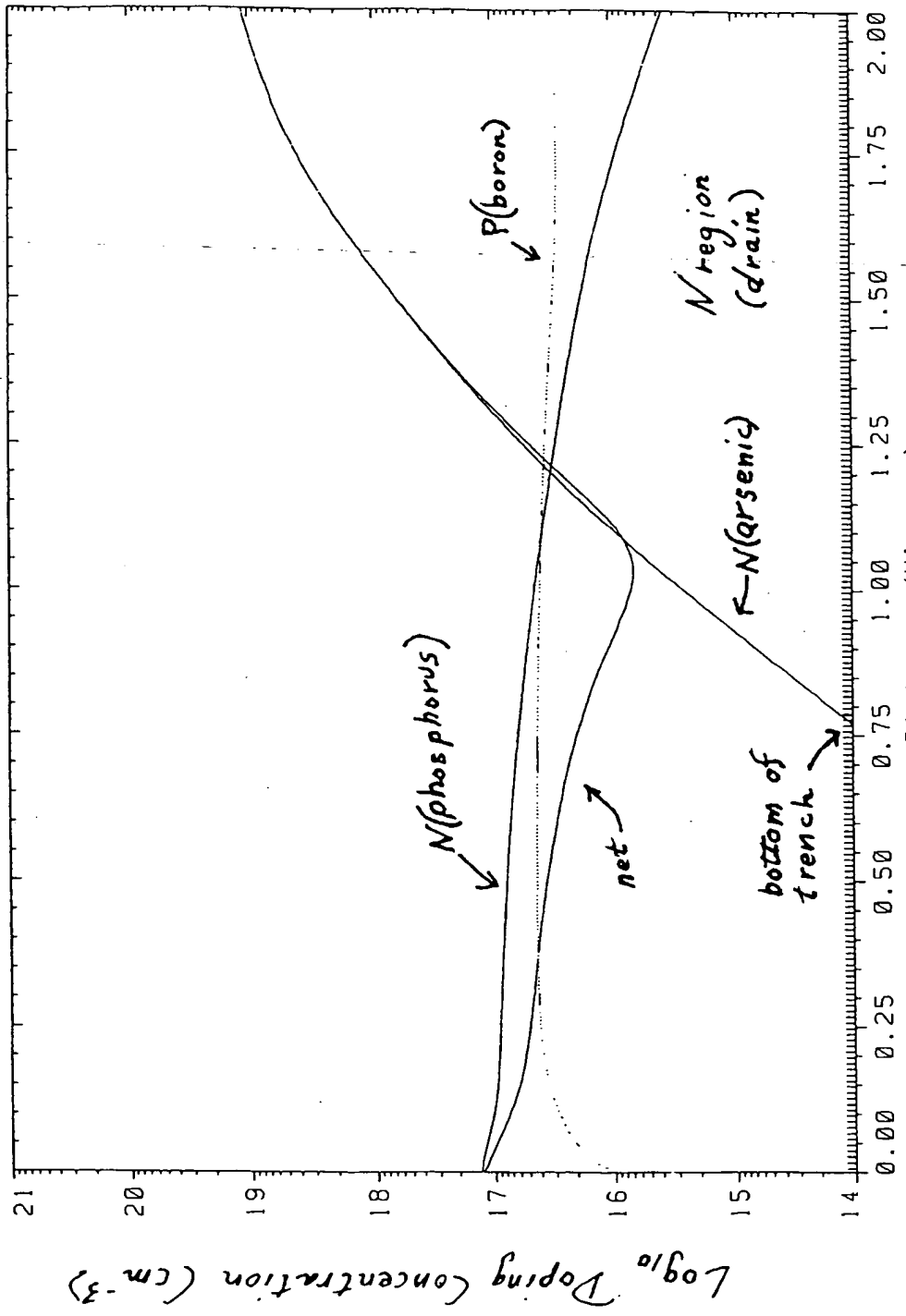
Log10 Doping Concentration (cm-3)
21
20
19
18
17
16
15
14
0.00
0.25
0.50
0.75
1.00
1.25
1.50
1.75
2.00
Distance (Microns)
P(boron)
N region (drain)
N(arsenic)
N(phosphorus)
net
bottom of trench

Fig. 8B

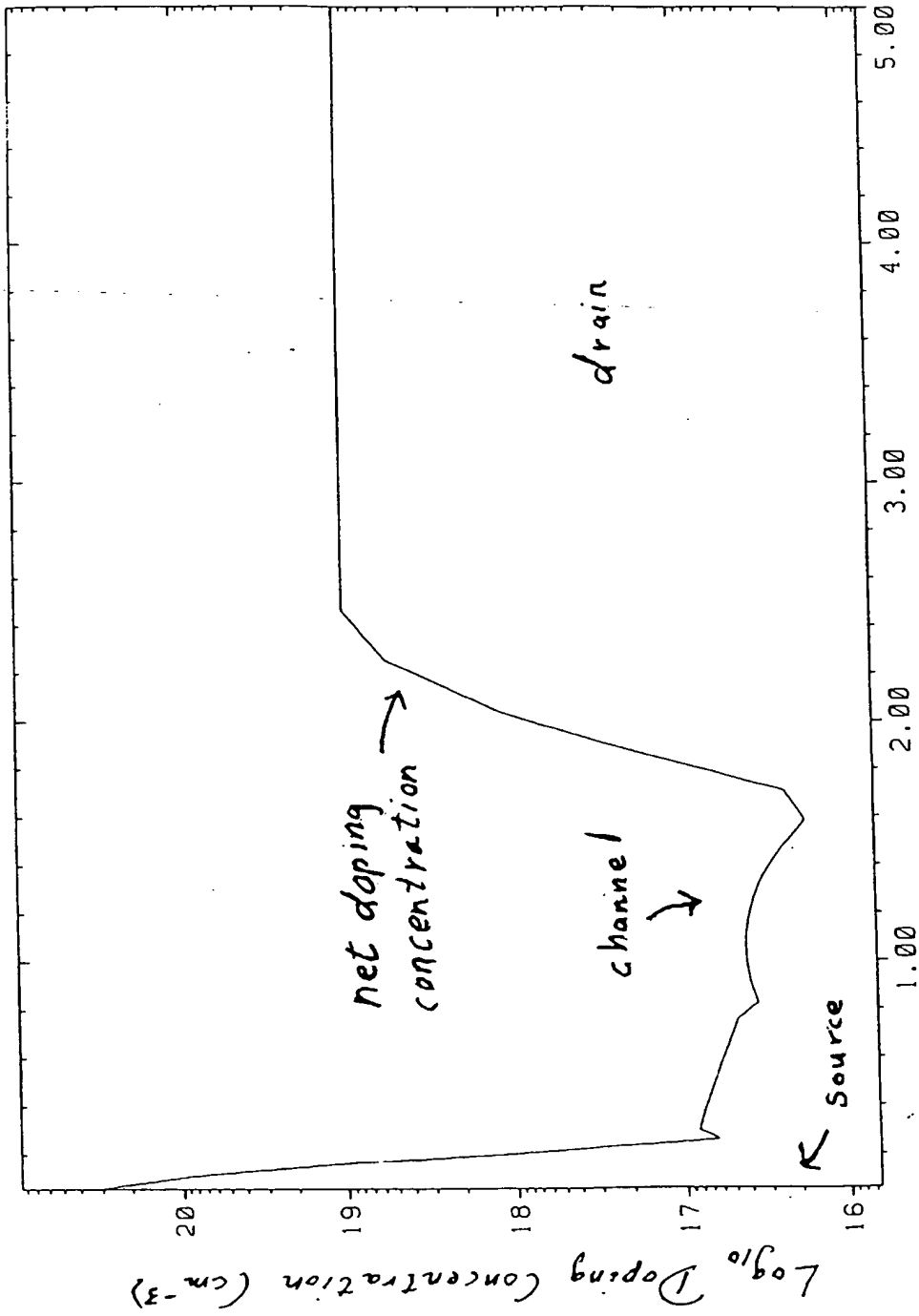

Fig. 9A

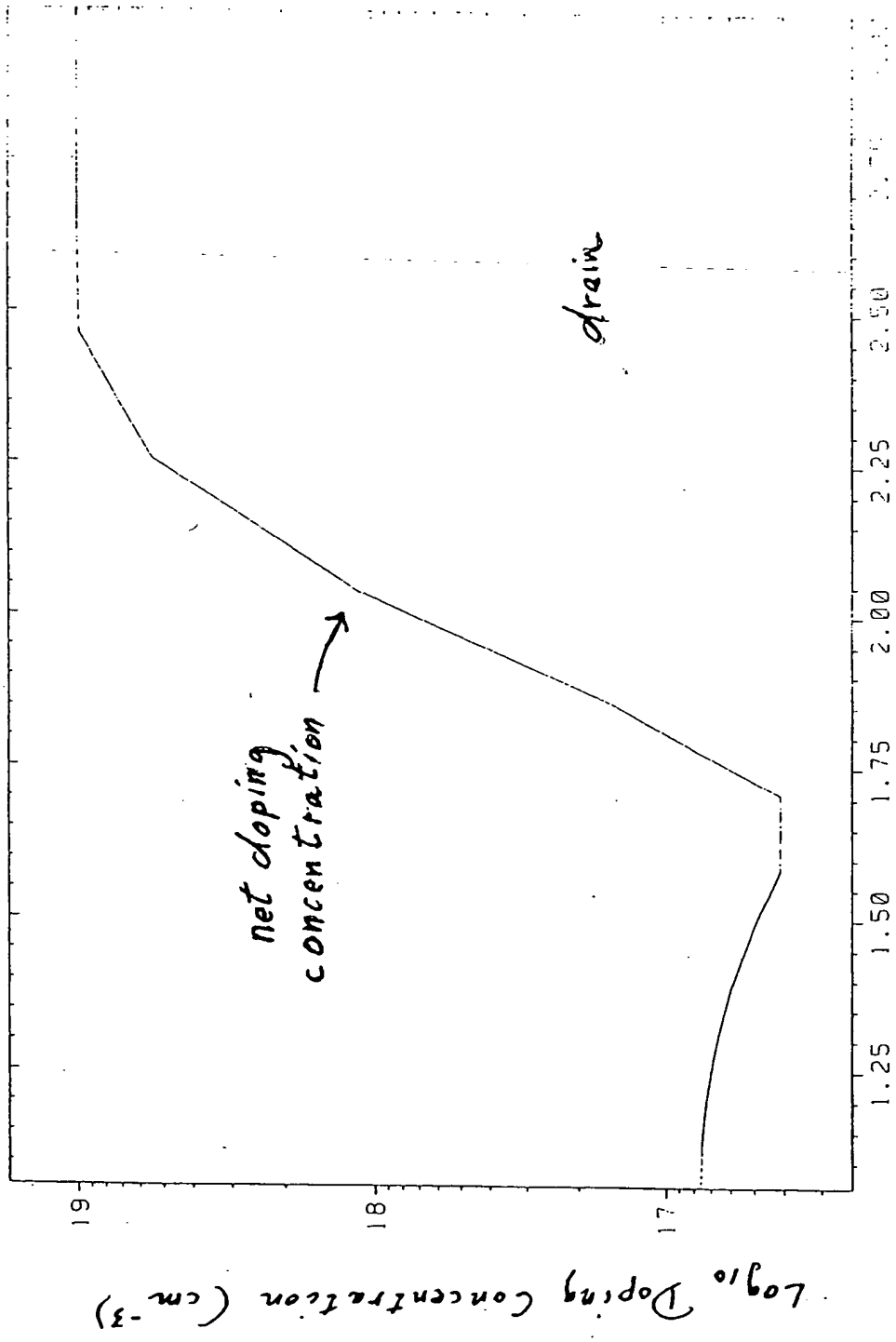
Log10 Doping Concentration (cm-3)
19
18
17
1.25
1.50
1.75
2.00
2.25
2.50
Distance (Microns)
drain
net doping concentration

Fig. 9B

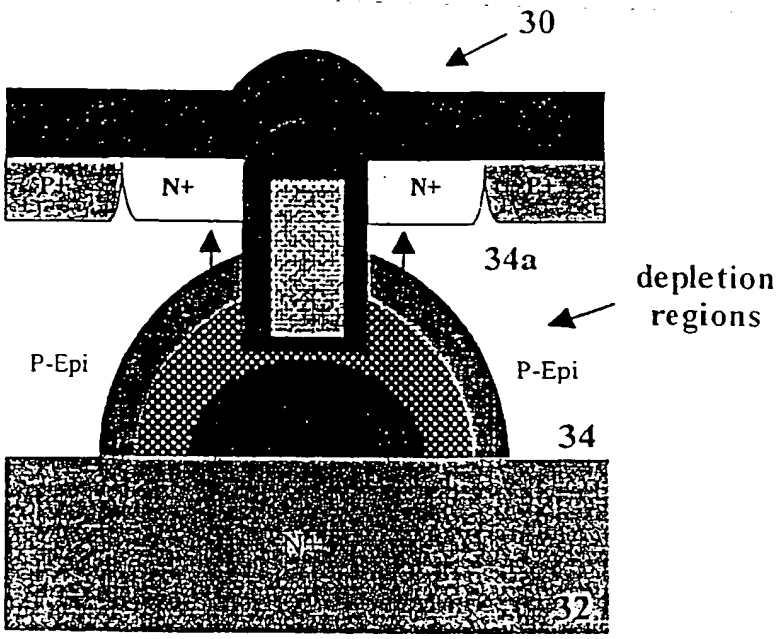

Figure 10

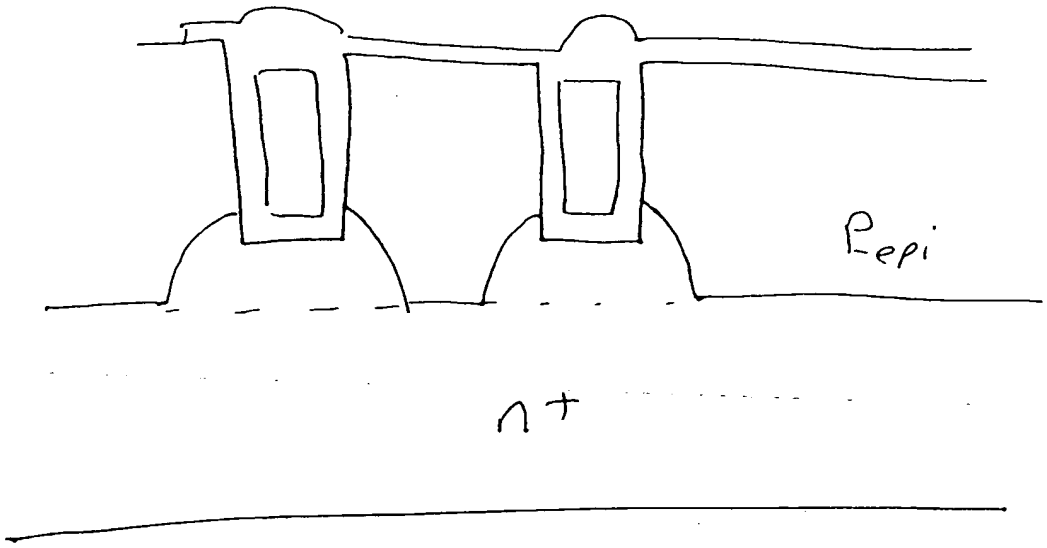

Fig. 11A

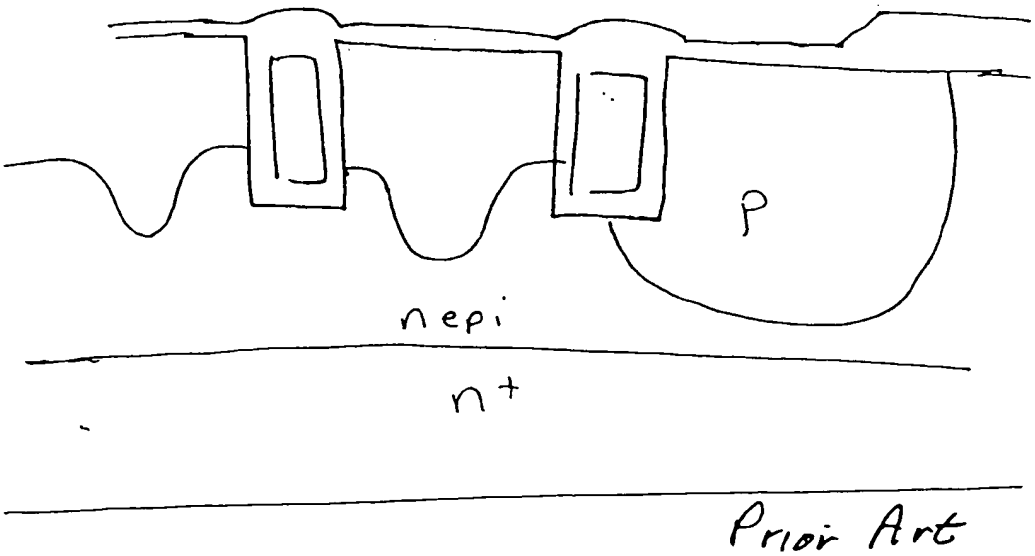

Fig. 11B

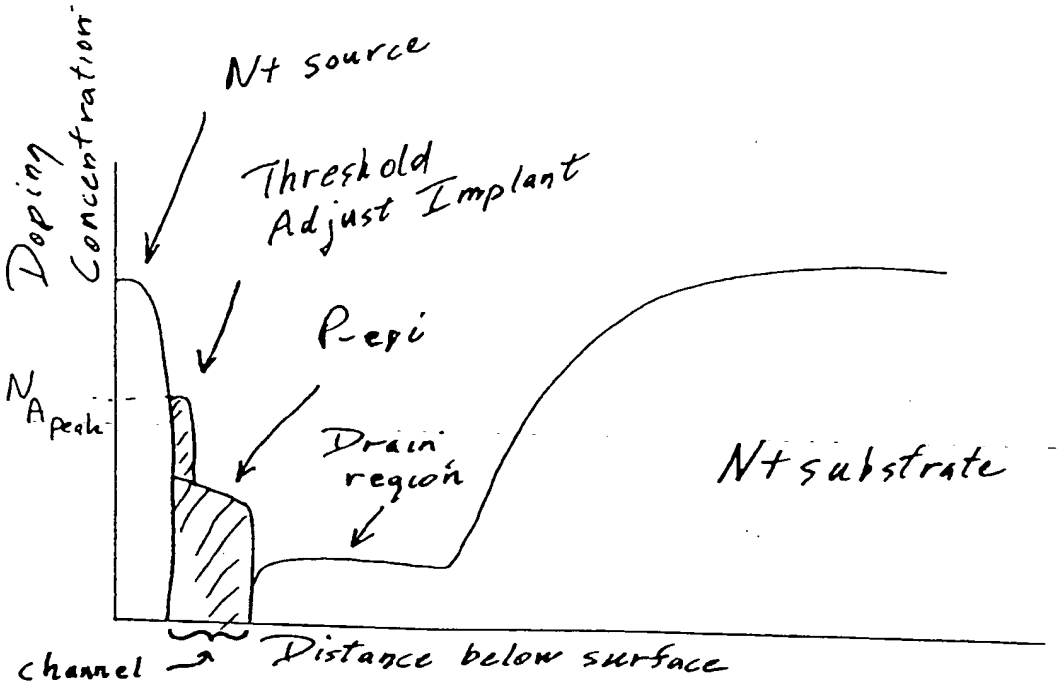

Fig. 12A

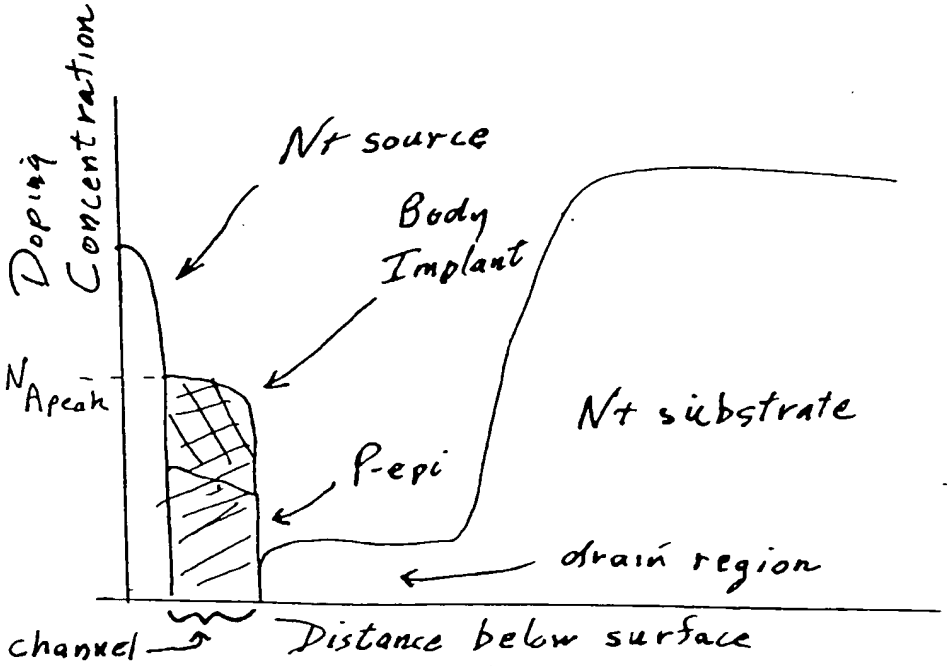

Fig. 12B

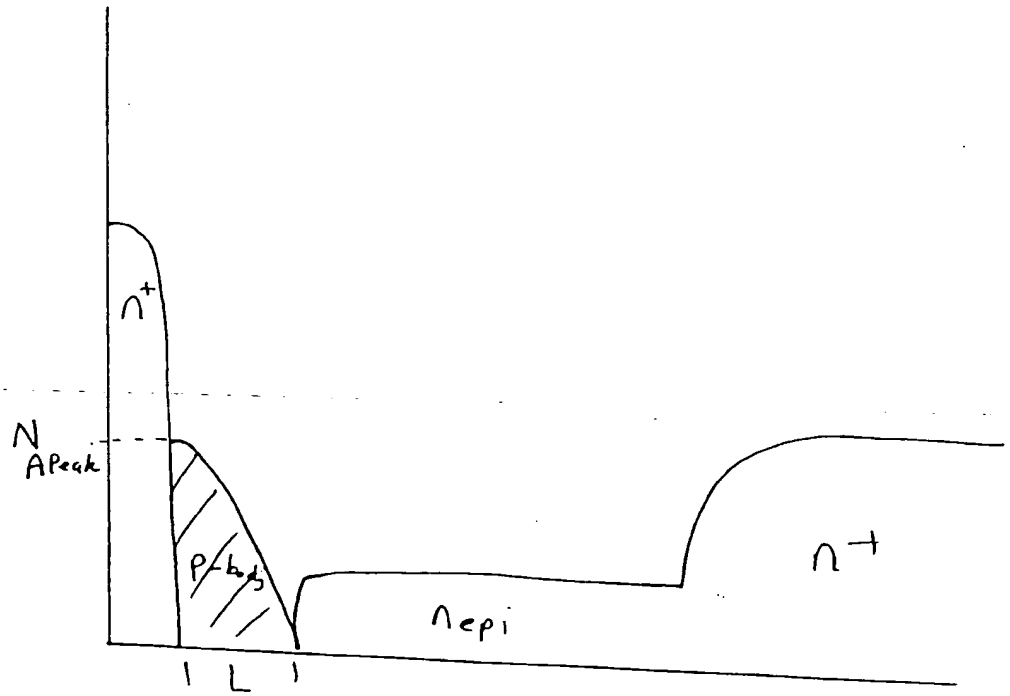

Fig. 13A

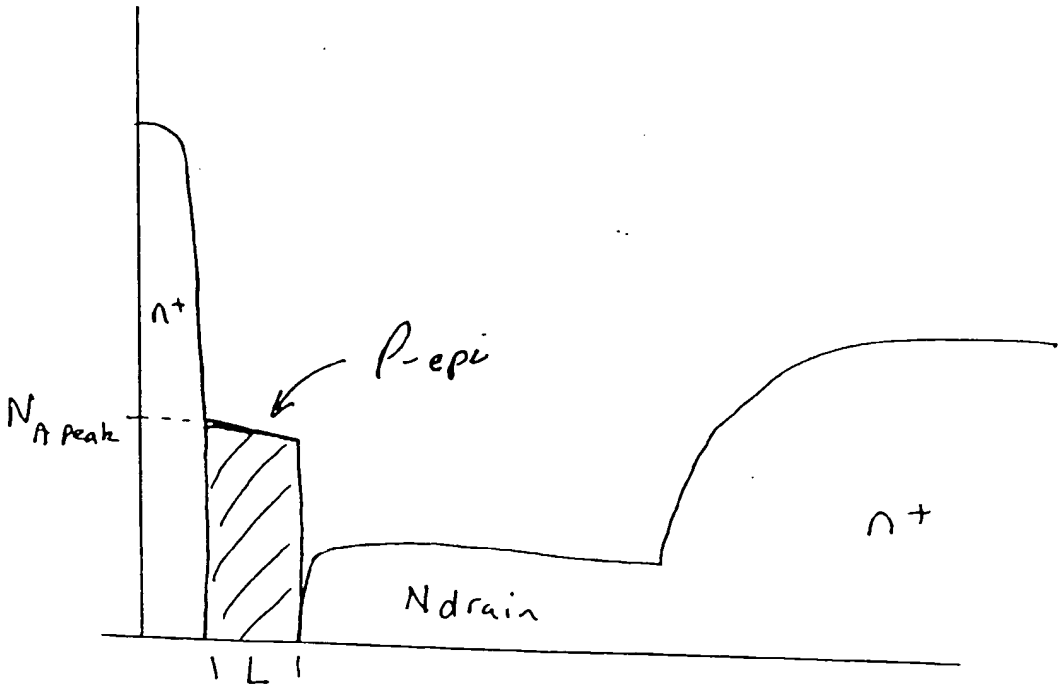

Fig. 13B

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European Patent Office
Office européen des brevets

(11) EP 1 014 450 A3

(12) EUROPEAN PATENT APPLICATION

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(43) Date of publication A2:
28.06.2000 Bulletin 2000/26

(21) Application number: 99106012.0

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(51) Int. Cl.[7]: H01L 29/78, H01L 21/336

(84) Designated Contracting States:
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Designated Extension States:
AL LT LV MK RO SI

(30) Priority: 25.11.1998 US 200197

(71) Applicant:
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Campbell, CA 95008 (US)

(74) Representative: Kolb, Georg
DaimlerChrysler AG,
Postfach 35 35
74025 Heilbronn (DE)

(54) Trench MOSFET having improved breakdown and on-resistance characteristics and process for manufacturing the same

(57) A trench MOSFET is formed in a structure which includes a P-type epitaxial layer overlying an N+ substrate. An N drain region is implanted through the bottom of the trench into the P-epitaxial layer, and after a diffusion step extends between the N+ substrate and the bottom of the trench. The junction between the N drain region and the P-epitaxial layer extends between the N+ substrate and a sidewall of the trench. In some embodiments the epitaxial layer can have a stepped doping concentration or a threshold voltage adjust implant can be added. Alternatively, the drain region can be omitted, and the trench can extend all the way through the P-epitaxial layer into the N+ substrate. A MOSFET constructed in accordance with this invention can have a reduced threshold voltage and on-resistance and an increased punchthrough breakdown voltage.

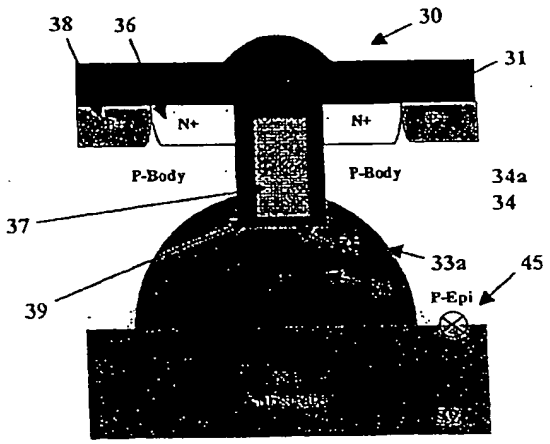

Figure 3

EP 1 014 450 A3

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 99 10 6012

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.7)
X	PATENT ABSTRACTS OF JAPAN vol. 018, no. 225 (E-1541), 22 April 1994 (1994-04-22) -& JP 06 021468 A (TOSHIBA CORP), 28 January 1994 (1994-01-28)	1-3,5,7, 12,13	H01L29/78 H01L21/336
Y	* abstract; figures 1-4 *	6,15-19	
X	US 5 216 275 A (CHEN XINGBI) 1 June 1993 (1993-06-01)	1-3,12, 13	
Y	* figure 4 *	15-19	
A	WO 98 04004 A (SILICONIX INC) 29 January 1998 (1998-01-29) * figures 3C,3D *	15-18	
Y	WO 98 12753 A (ADVANCED MICRO DEVICES INC) 26 March 1998 (1998-03-26) * figure 2A *	6,19	

TECHNICAL FIELDS SEARCHED (Int.Cl.7)

H01L

~~The present search report has been drawn up for all claims~~

Place of search	Date of completion of the search	Examiner
THE HAGUE	11 August 2000	GELEBART J.F.M.

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
A : technological background
O : non-written disclosure
P : intermediate document

T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

EPO FORM 1503 03.82 (P04C01)

European Patent Office

Application Number
EP 99 10 6012

CLAIMS INCURRING FEES

The present European patent application comprised at the time of filing more than ten claims.

☐ Only part of the claims have been paid within the prescribed time limit. The present European search report has been drawn up for the first ten claims and for those claims for which claims fees have been paid, namely claim(s):

☐ No claims fees have been paid within the prescribed time limit. The present European search report has been drawn up for the first ten claims.

LACK OF UNITY OF INVENTION

The Search Division considers that the present European patent application does not comply with the requirements of unity of invention and relates to several inventions or groups of inventions, namely:

see sheet B

☐ All further search fees have been paid within the fixed time limit. The present European search report has been drawn up for all claims.

☐ As all searchable claims could be searched without effort justifying an additional fee, the Search Division did not invite payment of any additional fee.

☐ Only part of the further search fees have been paid within the fixed time limit. The present European search report has been drawn up for those parts of the European patent application which relate to the inventions in respect of which search fees have been paid, namely claims:

☒ None of the further search fees have been paid within the fixed time limit. The present European search report has been drawn up for those parts of the European patent application which relate to the invention first mentioned in the claims, namely claims:

1-13,15-19

European Patent Office

LACK OF UNITY OF INVENTION
SHEET B

Application Number
EP 99 10 6012

The Search Division considers that the present European patent application does not comply with the requirements of unity of invention and relates to several inventions or groups of inventions, namely:

1. Claims: 1-13, 15-19

   Vertical MOSFET with a recessed gate. The body extends lower than the gate up to the drain and a drain extension extends between the drain and the bottom of the trench of the recessed gate. Method of manufacturing it.

2. Claim : 14

   Vertical MOSFET with a recessed gate. The body extends up to the drain and the bottom of the trench of the recessed gate extends into the drain.

ANNEX TO THE EUROPEAN SEARCH REPORT ON EUROPEAN PATENT APPLICATION NO. EP 99 10 6012

This annex lists the patent family members relating to the patent documents cited in the above-mentioned European search report. The members are as contained in the European Patent Office EDP file on
The European Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

11-08-2000

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
JP 06021468 A	28-01-1994	NONE	
US 5216275 A	01-06-1993	CN 1056018 A	06-11-1991
WO 9804004 A	29-01-1998	AU 3724197 A	10-02-1998
		EP 0948818 A	13-10-1999
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		EP 0931350 A	28-07-1999
		US 5960271 A	28-09-1999

EPO FORM P0459

For more details about this annex : see Official Journal of the European Patent Office, No. 12/82